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(54) **Multiple output switching power supply having one controlled output voltage and load compensation.**

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(73) Proprietor: **BULL HN INFORMATION SYSTEMS ITALIA S.p.A.**
Via Martiri d'Italia 3
I-10014 Caluso (Torino) (IT)

(72) Inventor: **Cavagnolo, Gian Paolo**
Via Caterina da Forli 28
I-20100 Milano (IT)
Inventor: **Scotti, Alessandro**
Via Genova 23
I-20010 Pregnana Milanese (IT)

(74) Representative: **Falcetti, Carlo et al**
c/o JACOBACCI & PERANI S.p.A.
Via Visconti di Modrone, 7
I-20122 Milano (IT)

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Description

The present invention relates to multiple output switching power supplies having one controlled output voltage.

Multiple outputs switching power supplies are known in which an unregulated DC voltage (obtained in case from a rectified AC voltage source) is periodically applied through switches to the primary winding of a transformer, so as to induce voltage pulses in a plurality of secondary windings.

The induced voltage pulses charge, through diodes, some capacitors connected to the output of the secondary windings.

The capacitors act as buffer filters and relatively constant DC voltages are available at their ends.

These voltage may be used to power loads.

By comparing the voltage available at the ends of one of such capacitors with a reference voltage, an error signal is obtained which is used to control, through suitable devices, the frequency and/or the duty cycle of the voltage and current pulses applied to the primary winding, so as to regulate the voltage at the terminals of one capacitor, thus of one output.

Missing any independent control circuit for the other outputs, the charge voltage of the other capacitors, hence the voltage available at the other outputs, is indirectly regulated and is largely affected by the load conditions of the several outputs both in static as well as transient situations.

To overcome this disadvantage several solutions are known.

They will be detaily considered in the following but in any event they are not completely satisfactory, particularly in dynamic conditions of load variation.

One of these solutions, known for instance from GB-A-2166270, provides for a series connection among outputs and requires the use of components sized to substain the sum of the loads connected to the outputs.

In addition the voltage ripple which affects the indirectly regulated output is the sum of the intrinsic ripple voltage and the one affecting the regulated output.

Further in case of transient load peaks at the regulated output, a relevant voltage drop occurs at the indirectly regulated output. These drawbacks are overcome by the multiple output power supply of the invention where the filter and buffer capacitance of a first regulated voltage output, higher than a second voltage of a second unregulated output, is comprised of two series connected capacitors.

The capacity of the two capacitor is selected so as to obtain, at the connection node of the two capacitors, a voltage equal to or sligthly higher than the voltage at the second output.

The node connecting the two capacitors is connected to the second output through a diode which enables power flowing from one of the capacitors to the second output if the voltage at the second output decreases.

The diode prevents coupling of the outputs if the voltage at the regulated output decreases, due to load peaks.

The features and the advantages of the invention will appear more clearly from the following description of a preferred form of embodiment and from the enclosed drawings where:

- Figure 1 is a block diagram of a first multiple output power supply known from the prior art.
- Figure 2 is a block diagram of a second multiple output power supply known from the prior art.
- Figure 3 is a block diagram of a preferred form of embodiment of a multiple output power supply according to the present invention.

Figure 1 shows a multiple output power supply known from the prior art. An unregulated DC voltage +V is input to a terminal of a primary winding 1 of a transformer T.

The other terminal is periodically connected to ground through a switching transistor 2.

Two secondary windings 3,4 of the transformer are series connected each to the other.

A terminal 5 of secondary winding 3 is grounded.

Node 6, common to the two secondary windings, is connected to the anode of diode 7, whose cathode is connected to an output terminal U2.

A capacitor 8 is connected between terminal U2 and ground.

The terminal 9 of secondary winding 4 is connected to the anode of a diode 10, whose cathode is connected to an output terminal U1.

A capacitor 11 is connected between U1 and ground.

The voltage/current pulses induced in the secondary windings 3,4 charge the capacitors at a voltage level V1,V2, respectively appearing between output terminals U1,U2 and ground.

A comparator circuit 12 receives voltage V1, compares it with a reference voltage and generates an error signal ERR, which is forwarded to a control logic 13.

The control logic 13 applies a control signal to the base of transistor 2.

This signal controls the frequency or the duty cycle of the voltage pulses applied to the primary winding thus regulating voltage V1 at a predetermined value.

It is clear that for predetermined load conditions L1,L2 on the outputs the ration V1/V2 between the two output voltages is equal to the ration between the turn number of the secondary winding 3 and the sum of the turn numbers of the windings 3 and 4.

Therefore voltage V2 is indirectly regulated.

However if the load L1 decreases below a predetermined value, whilst load L2 is not changed, voltage

V2 drops below the indirect regulation value.

At the extreme, if load L1 is zero and power waste in the components is neglected, no power has to be transferred to capacitor 11 and the frequency or the duty cycle of the voltage pulses induced in the secondary windings must virtually drop to zero.

As a consequence voltage V2 virtually drops to zero.

By reverse V2 largely rises above a nominal indirect regulation value if L2 decreases (at load L1 non zero).

Normally a power supply as the described one finds use in equipments where the loads powered by the two outputs are relatively constant. Power supplies of this kind are also used in data processing system peripheral units, such as printers, diskette drivers, and like.

In these units the voltage V2, of low value and generally of +5V, is used to power a relatively constant load consisting in logic control circuits.

Voltage V1, having an higher value and tipically comprised between +15 and +40 V, is used to feed power devices such as motors and electromagnetic actuators, which constitute broadly variable loads.

In this case and in order to avoid broad changes in voltage V2 depending on load L1, it is essential to assure that L1 is kept relatively constant.

This is obtained by connection of a fixed resistive load R1 between terminal U1 and ground, so that the relative change of the total load R1+L1 is contained within acceptable limits.

It is clear that such arrangement reduces the efficiency of the power supply, requires an oversizing and causes power waste and development of heat which must be dissipated.

Figure 2 shows a second arrangement known from the prior art, which provides a partial solution of the problem.

Since this arrangement is very similar to the one shown in fig. 1 equivalent elements in both figures are referenced with the same numerals.

In figure 2 terminal 5 of secondary winding 3 is grounded.

The other terminal 14 is connected to the anode of diode 7, whose cathode is connected to terminal U2. A capacitor 8 is connected between U2 and ground.

Terminal 15 of secondary winding 4 is connected to U2.

The other terminal 9 is connected to the anode of diode 10, whose cathode is connected to output terminal U1.

A capacitor 16 is connected between terminals U1,U2.

The voltage V1, available between terminal U1 and ground is the sum of the charging voltage of the two capacitors 16,8 and is input to comparator 12.

Even in this case voltage V1 is directly regulated and voltage V2 is indirectly regulated.

By this arrangement the two outputs are dynamically coupled: every change in voltage V2 affects voltage V1 too so that the indirect regulation is more effective.

As a drawback, the diode 7 must supply the full current required to feed both load L2 both load L1. Therefore it must be largely sized. Further the output U2 is affected by the ripple voltage due to the impulsive loading of capacitor 8 and in addition by the whole ripple voltage affecting ouptut U1 (capacitor 8 receives power needed by load L1 and transfers such power to load L1).

This ripple voltage may be unacceptable if, as it is often the case, most of the power must be supplied to output U1, which is at a voltage higher than V2.

A ripple voltage in the order of 5% at an output averaging 30 V (equal to 1,5V in absolute value), when transferred to an output averaging 5V, results in a ripple voltage in the order of 30% hence unacceptable.

A further inconvenient occurs in case power peaks are drain from output U1, which peaks may exceed the maximum regulating range of the power supply.

Temporary overloads are a normal event in the operation of computer peripheral units because it is against economy to size a power supply in order to perform regulation even in case of temporary overloading.

In these circumstances, voltage V1 may fall well below the normal regulation value and causes a corresponding decrease of voltage V2.

If the decrease of V1 may be tolerated, the decrease in V2 may hamper the correct operation of the logical circuits.

These drawbacks are overcome by the embodiment of Fig. 3, where the elements functionally equivalent to the ones of the preceding figures are referenced by the same numbers.

In Fig. 3 the secondary winding 3 is series connected to secondary winding 4 (as in Fig. 1).

The terminals 5 of secondary winding 3 is grounded and the common node of the two secondary windings is connected to the anode of a diode 7, whose cathode is connected to output U2.

A capacitor 8 is connected between U2 and ground.

The terminal 9 of secondary winding 4 is connected to the anode of diode 10, whose cathode is connected to the output terminal U1. A capacitive element consisting in two series connected capacitors 17,18 is connected between terminal U1 and ground.

Voltage V1, available between terminal U1 and ground is input to comparator circuit 12, which forwards an error signal to the control circuits 13 of the switching transistor 2.

Even in this case voltage V1 is directly regulated

and voltage V2 is indirectly regulated.

The node 19, common to the two capacitors 17,18 is connected to the anode of a diode 20, whose cathode is connected to terminal U2.

The capacitance of the two capacitors 17 and 18 is selected so that the voltage at node 19 is equal or slightly higher than voltage V2.

This result can be easily obtained because is well known that a charging voltage applied to two series connected capacitors is distributed between the two capacitor so that the ration of the charge voltages is inversely proportional to the ration of the respective capacitances.

In this way, even if no load L1 or a minimum load L1 is connected to output U1, any voltage decrease at terminal U2 causes the forward biasing of diode 20 and a current flow from node 19 which tends to discharge capacitor 18, thus decreasing the value of V1.

In other words a fraction of the power required by load L2, which is not supplied by capacitor 8, is supplied by capacitor 18 which sustains voltage V1 and causes the intervention of the control circuits, which increase the power transferred from primary to secondary windings, in order to keep voltage V1 at the regulation level.

Diode 7 may be sized to sustain the maximum load L2 and is not required to sustain in addition the maximum load L1 as in case of Fig. 2.

Moreover the ripple voltage of U1 is transferred to output U2 at a reduced extent only.

First because only a fraction of the ripple voltage equal to the ration between the voltage at node 12 (≃V2) and voltage V1 is applied to the anode of diode 20 and second because this fraction is largely clipped by the diode (as a limit, when the diode is non conductive the filtering it total).

In case of temporary overload at output U1 and V1 voltage drop as to regulation value, diode 20 is reverse biased and no energy trasfer occurs from capacitor 8 towards capacitor 18.

Therefore V2 does not collapses.

It must be noted that voltage at node 19, relative to voltage V1 is univocally defined by the capacitance of capacitors 17,18 only in case of perfect capacitors.

In practice, real capacitors always exhibit a small leakage current and act as perfect capacitors having a resistance in parallel.

This fact may cause a drift of the voltage at node 19.

To prevent node 19 from dropping below a predetermined voltage value V2 it is possible to connect a resistor 21 in parallel to capacitor 17. The value of such resistor which may be very hight, is selected so that the voltage applied to its terminals causes a current flow having the same order of magnitude of the maximum foreseable leakage current of capacitor 18.

In this way voltage at node 19 is certainly kept at the level of voltage V2, plus the voltage drop in diode 20, except in case of transient overloads.

It is clear that the preceding description relates to a preferred embodiment and that several changes can be made.

In particular the circuits which convert an unregulated DC voltage in voltage pulses applied by means of a transformer to two filtering buffer elements which sustain the voltage at two outputs are examples only.

It is clearly possible to use control circuits which apply voltage pulses of opposite value to the primary winding of a transformer. It is also possible to apply voltage pulses of opposite direction to either one or the other of two primary windings depending on the direction of the pulses.

In both cases voltage pulses of opposite polarity are obtained at the secondary windings.

These pulses may be rectified with diode bridges and may be input to output filtering and buffering capacitors.

As in the case of the primary winding the secondary windings too may consists in two half windings coupled to diode half-bridges for rectifying the voltage pulses of opposite polarity induced in the half windings and for inputting them to the output filtering capacitors. Therefore the invention may be used in all kind of power supplies where voltage pulses input to a transformer primary winding induce voltage pulses in secondary windings, the induced voltage pulses charging at least two capacitive filtering elements which sustain two distinct output voltages, one of which provides a feedback signal for controlling parameters of the input pulses, such as frequency and/or duty cycle, thus achieving regulation of one of the two output voltages.

It is also clear that even if reference has been made, in the description, to positive voltages, the invention may be used even in case of negative voltages, by reversing the conductive direction of the diodes in the circuit.

Claims

1. Multiple output switching power supply providing a first directly controlled output voltage (V1) between a first output (U1) and ground and indirect control of at least a second output voltage (V2) between a second output (U2) and ground, comprising a trasformer (T) having at least a primary winding (1) series connected to a controllable switch for periodical connection to a voltage source (+V) and at least two secondary windings (3,4) periodical voltage pulses being induced in said secondary windings (3,4), said voltage pulses loading, through rectifying elements (7,10), a first capacitive element (17,18) having a grounded terminal, at a first voltage V1 and a second capacitive element (8), having a grounded terminal,

at a second voltage V2, equal in sign to V1 but having a lower value, said voltage being available, for loads powering, respectively ai said first output and at said second output,
characterized in that said first capacitive element (17,18) comprises a first (17) and a second (18) capacitor, series connected between said first output U1 and ground, the node (19) common to said first and second capacitor being connected to said second output (U2) through a diode (20), said first (17) and second (18) capacitors having a value such that said first voltage (V1) applies to said node (19) a voltage level equal or slightly higher, in absolute value, than said second voltage (V2), said diode (20) being conductive in the direction which allows power flow from said first capacitive element (17,18) to said second output terminal (U2) and said second capacitive element (8).

2. Power supply as in claim 1 comprising a resistor (21) connected between said first output (U1) and said node (19) common to said first and second capacitor.

Patentansprüche

1. Schaltnetzteil mit Mehrfachausgang, das eine erste direkt geregelte Ausgangsspannung (V1) zwischen einem ersten Ausgang (U1) und Masse und eine indirekte Regelung wenigstens einer zweiten Ausgangsspannung (V2) zwischen einem zweiten Ausgang (U2) und Masse erzeugt, das einen Transformator (T) mit wenigstens einer Primärwicklung (1), die in Reihe mit einem regelbaren Schalter zur periodischen Verbindung mit einer Spannungsquelle (+V) geschaltet ist, und wenigstens zwei Sekundärwicklungen (3,4) umfaßt, wobei periodische Spannungsimpulse in den Sekundärwicklungen (3,4) induziert werden, wobei die Spannungsimpulse über Gleichrichterelemente (7,10) ein erstes kapazitives Element (17,18) mit einem geerdeten Anschluß bei einer ersten Spannung V1 laden und ein zweites kapazitives Element (8) mit einem geerdeten Anschluß bei einer zweiten Spannung V2 laden, die das gleiche Vorzeichen wie V1, jedoch einen niedrigeren Wert hat, wobei die Spannung zur Lastspeisung am ersten Ausgang bzw. am zweiten Ausgang zur Verfügung steht,
dadurch gekennzeichnet, daß das erste kapazitive Element (17,18) einen ersten (17) und einen zweiten (18) Kondensator umfaßt, die in Reihe zwischen den ersten Ausgang U1 und Masse geschaltet sind, wobei der Knoten (19), den der erste und der zweite Kondensator gemeinsam haben, über eine Diode (20) mit dem zweiten Ausgang (U2) verbunden ist, wobei der erste (17) und der zweite (18) Kondensator einen Wert haben, der so liegt, daß die erste Spannung (V1) an den Knoten (19) einen Spannungspegel anlegt, der hinsichtlich des absoluten Wertes genauso groß ist wie oder etwas größer als die zweite Spannung (V2), wobei die Diode (20) in der Richtung leitend ist, die Spannungsfluß vom ersten kapazitiven Element (17,18) zum zweiten Ausgangsanschluß (U2) und zum zweiten kapazitiven Element (8) ermöglicht.

2. Netzteil nach Anspruch 1, das einen Widerstand (21) umfaßt, der zwischen den ersten Ausgang (U1) und den Knoten (19) geschaltet ist, den der erste und der zweite Kondensator gemeinsam haben.

Revendications

1. Alimentation à découpage à sorties multiples fournissant une première tension de sortie directement régulée (V1) entre une première sortie (U1) et la masse et la régulation indirecte d'au moins une seconde tension de sortie (V2) entre une seconde sortie (U2) et la masse, comprenant un transformateur (T) ayant au moins un enroulement primaire (1) connecté en série à un commutateur pouvant être commandé pour la connexion périodique à une source de tension (+V) et des impulsions de tension périodiques d'au moins deux enroulements secondaires (3, 4) étant induites dans lesdits enroulements secondaires (3, 4), lesdites impulsions de tension chargeant, par l'intermédiaire d'éléments de redressement (7, 10), un premier élément capacitif (17, 18) ayant une borne à la masse, à une première tension V1 et un second élément capacitif (8), ayant une borne à la masse, à une seconde tension V2, de même signe que V1 mais ayant une valeur inférieure, ladite tension étant disponible, pour l'alimentation de charges, respectivement à ladite première sortie et à ladite seconde sortie, caractérisé en ce que ledit premier élément capacitif (17, 18) comporte un premier (17) et un second (18) condensateurs, connectés en série entre ladite première sortie U1 et la masse, le noeud (19) commun auxdits premier et second condensateurs étant connecté à ladite seconde sortie (U2) par l'intermédiaire d'une diode (20), lesdits premier (17) et second (18) condensateurs ayant une valeur telle que ladite première tension (V1) applique audit noeud (19) un niveau de tension égal ou légèrement supérieur, en valeur absolue, à ladite seconde tension (V2), ladite diode (20) étant conductrice dans un sens qui permet la circulation du flux d'énergie depuis ledit premier

élément capacitif (17, 18) vers ladite seconde borne de sortie (U2) et ledit second élément capacitif (8).

2. Alimentation selon la revendication 1 comprenant une résistance (21) connectée entre ladite première sortie (U1) et ledit noeud (19) commun auxdits premier et second condensateurs.

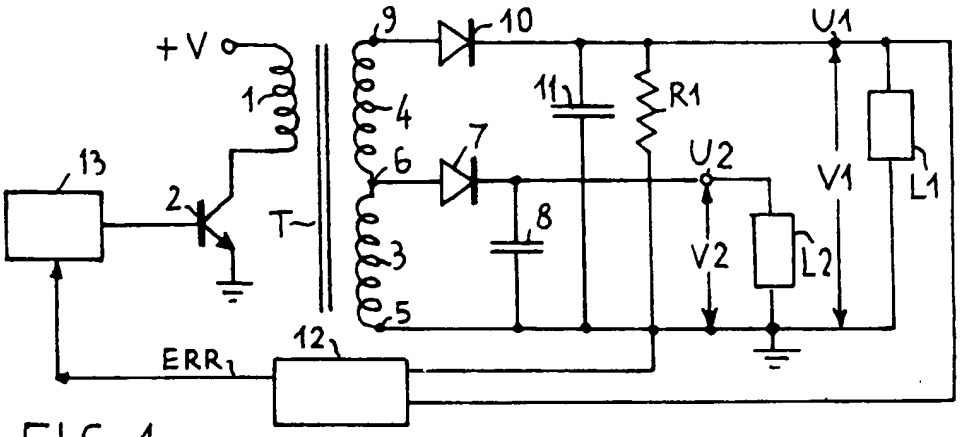

FIG.1

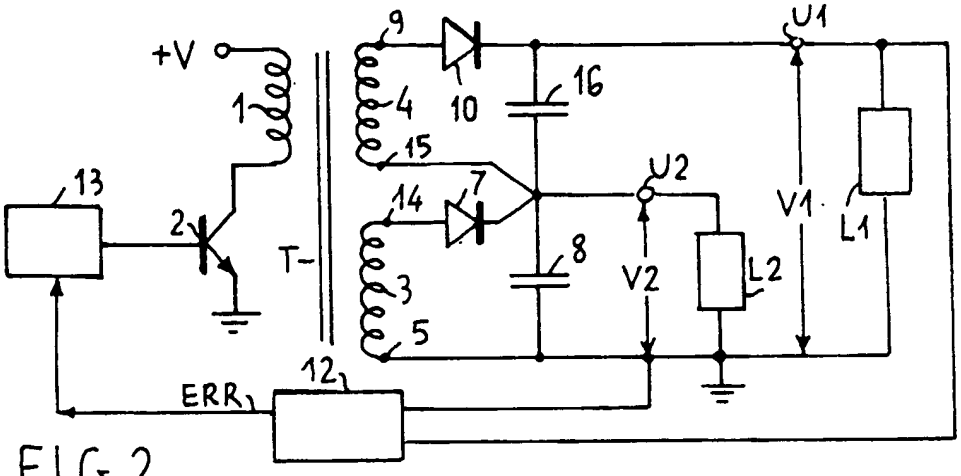

FIG.2

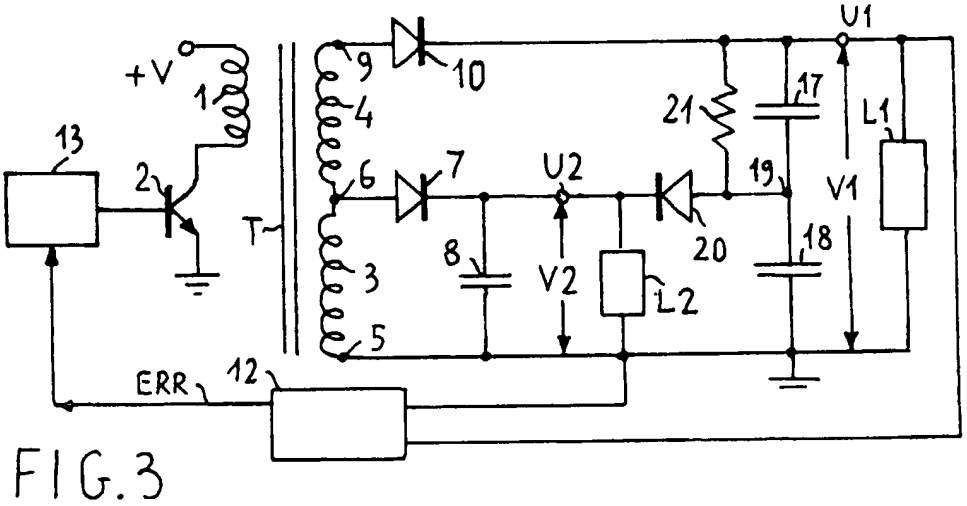

FIG.3